MAY 27 2003
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PATENT & TRADEMARK OFFICE

Attorney Docket 040301/0578

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#24 MY 9 attn

Applicant: Nobutoshi AOKI et al.

Title: SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING INSULATED GATE FIELD EFFECT TRANSISTOR AND METHOD OF MANUFACTURING THE SAME

Appl. No.: 09/440,928

Filing Date: November 16, 1999

Examiner: S. Rao

Art Unit: 2814

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PROPOSED CHANGES TO THE DRAWINGS AND SUBMISSION OF CORRECTED FORMAL DRAWINGS

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

Applicants propose to amend FIG 3 as shown in red on the attached copy of the drawing. A corrected formal drawing showing FIGS. 3(A) and 3(B) is also attached herewith.

Respectfully submitted,

Aaron C. Chatterjee

May 27, 2003 (Tuesday after holiday)
Date

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